

## 5 TRANSISTOR AMPLIFYING CIRCUIT

### 5.1 Objectives

- Understanding the basic characteristics of an amplifying circuit.
- Understanding the load line analysis of a transistor amplifier.

### 5.2 Basic Description

#### 5.2.a New Terminology

##### (1) CE Amplification:

CE is the abbreviation of common emitter. The related circuit is called common-emitter amplifier.

##### (2) CC Amplification:

CC is the abbreviation of common collector. The related circuit is called common-collector amplifier, also called emitter follower.

##### (3) CB Amplification:

CB is the abbreviation of common base. The related circuit is called common-base amplifier.

##### (4) Saturation:

When the input current ( $I_b$ ) of the transistor is increased but the current in the output circuit is not increased accordingly (in other words,  $I_c \neq \beta I_b$ ), CE of the transistor is similar to short circuit at this time. The magnitude of  $I_c$  will be determined by  $V_{cc}$  and the resistance of the output circuit.

##### (5) Cutoff:

Input current of the transistor is zero, and its output current is also zero. In other words, two terminals of CE is not conducted, and is similar to open circuit.

##### (6) Active Region:

The operation of the transistor is neither in saturation region nor in cutoff region. Two terminals of GE are neither short-circuit nor open-circuit, and its function is similar to a variable resistor controlled by the input current. Saturation, cutoff and active regions are the three modes of operation of the transistor.

##### (7) DC Bias:

The DC voltage or current required for the transistor to operate in saturation, cutoff or active region.

##### (8) $h_{fe}$ .

The current amplification factor of CE configuration (under small signal).

##### (9) $h_{fb}$ :

The current amplification factor of CB configuration (under small signal).

##### (10) $h_{ie}$ :

The  $Z_i$  (input impedance) of CE configuration.

(11) **h<sub>ib</sub>**:

The Z<sub>i</sub> of CB configuration.

(12) **h<sub>re</sub>**:

The reverse voltage ratio of CE configuration.

(13) **h<sub>rb</sub>**:

The reverse voltage ratio of CB configuration.

(14) **h<sub>oe</sub>**:

Output transconductance of CE configuration.

(14) **h<sub>ob</sub>**:

The output transconductance of CB configuration.

### 5.2.b Basic Principle

Depending on the grounding status of the transistors, the basic amplifying circuits can be classified into the following three configurations:

- CE amplification
- CC amplification
- CB amplification.

Among them the CE configuration is the most commonly used mode which will be introduced as follows:

#### CE Amplifier

The basic circuit of CE amplifier is shown in Fig 5.1, wherein the input signal and the output signal share the common E. In other words, E is utilized as the common point which is conventionally called "ground", and is expressed as or. This is actually used as a common terminal in the circuit, and is different from the "ground" defined in the electrical circuit. In the actual circuit, the coexistence of V<sub>bb</sub> and V<sub>cc</sub> is not economic and not practical. One power supply V<sub>cc</sub> is usually provided for both I<sub>b</sub> and I<sub>c</sub>. A typical circuit is shown in Fig 5.2.

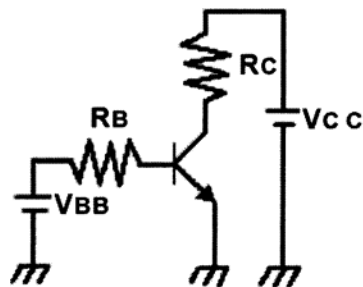


Fig. 5.1

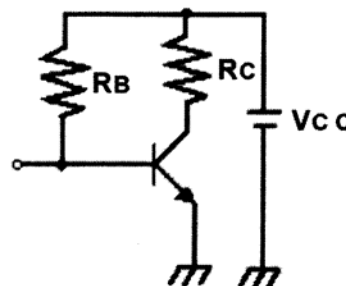


Fig. 5.2

#### Bias Arrangement for CE Amplifier

- 1) Fixed bias circuit.

2) DC bias circuit independent of  $\beta$  value (also called self-bias).

In order to increase the stability of the circuit, the above bias circuits have been improved to: the fixed bias circuit with emitter resistance and collector-feedback bias circuit. The basic principle for the commonly used bias arrangement is described as follows:

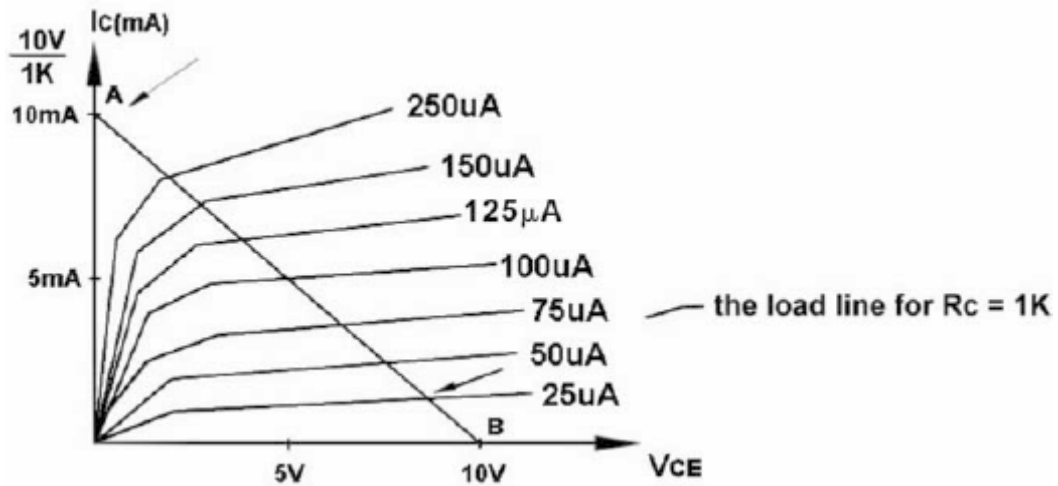
**A. Fixed bias circuit**

☞ Find out DC load line (DC bias). As shown in Fig 5.2, where  $\beta = 50$  and

- $I_b = \frac{V_{cc} - V_{be}}{R_s} = \frac{10V - 0.6V}{100K} = \frac{9.4}{100K} \cong 100\mu A$
- $I_c = \beta I_b = 50 \times 100 \mu A = 5000 \mu A = 5mA$
- $V_{ce} = V_{cc} - I_c R_c = 10V - 5mA \times 1K = 5V$

This can be expressed in the output characteristic curve shown as follows:

The line connected between the coordinates (0,  $V_{cc}/R_c$ ) and ( $V_{cc}$ , 0) is referred to as load line.



**Fig. 5.3**

- Q is called operating point.
- When the transistor of this circuit is saturated,  $I_c = V_{cc}/R_c$  and  $V_{ce} = 0$  (point A). When the transistor is cut off,  $I_c = 0$  and  $V_{ce} = 12V = V_{cc}$  (point B).
- The operating point of this circuit is set at  $I_c = 5.7mA$  and  $V_{ce} = 6.3V$ . The transistor is thus operated in active region.

☞ Operation status with AC signal input

From the DC load line we can find that the maximum of  $V_o(=V_{ce})$  is  $V_{cc}$  ( $=10V$ ), and the minimum of  $V_o$  is  $0V$ , with the variation range from  $0-10V$ . In other words, the variation of  $V_o$  is between  $0V$  and  $10V$ , regardless of the variation of input signal.

- As shown in Fig 5.2,  $R_c = 1K$ ,  $R_b = 100K$ ,  $\beta$  of the transistor = 50, then the  $\pm 50$   $\mu A$  AC current is applied to the input terminal. As shown in Fig 5.3, after the DC load line is plotted, we can find out that  $I_b$  of Q point is  $100 \mu A$ . The variation range of the input current is therefore between  $50 \mu A$  and  $150 \mu A$ .

If  $I_b = 50 \mu A$ ,

$$I_c = \beta \times I_b = 50 \times 50 \mu A = 2.5mA$$

$$V_{ce}: V_{cc} - I_c \times R_c = 10V - (2.5mA \times 1K) = 7.5V$$

If  $I_b = 150 \mu A$ ,

$$I_c = \beta \times I_b = 50 \times 150 \mu A = 7.5mA$$

$$V_{ce} = V_{cc} - I_c \times R_c = 10V - (7.5mA \times 1K) = 2.5V$$

The relation between  $V_o$  ( $V_{ce}$ ) and  $I_b$  corresponding to  $I_b$  is shown in Fig 5.4. ( $V_{cc}=20 V$ ,  $R_c=10 K$ ,  $V_{CE-Q}=10 V$ )

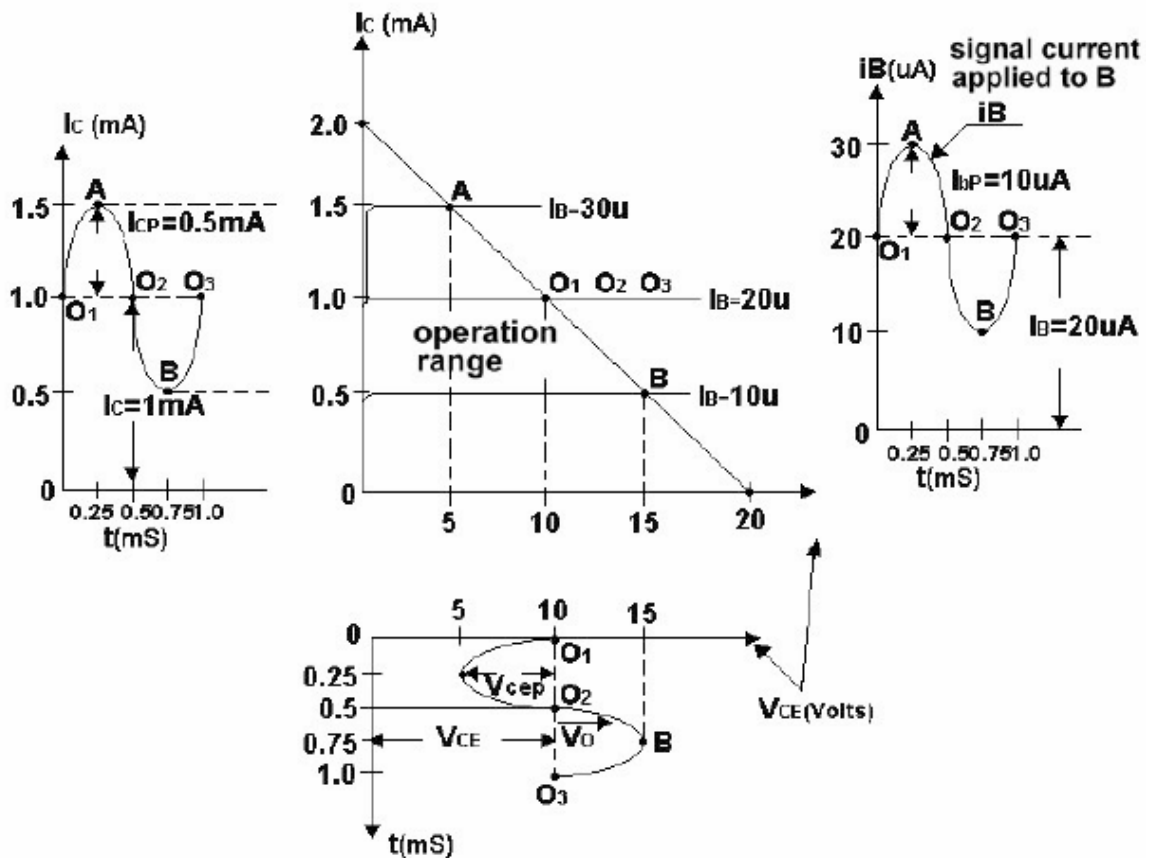
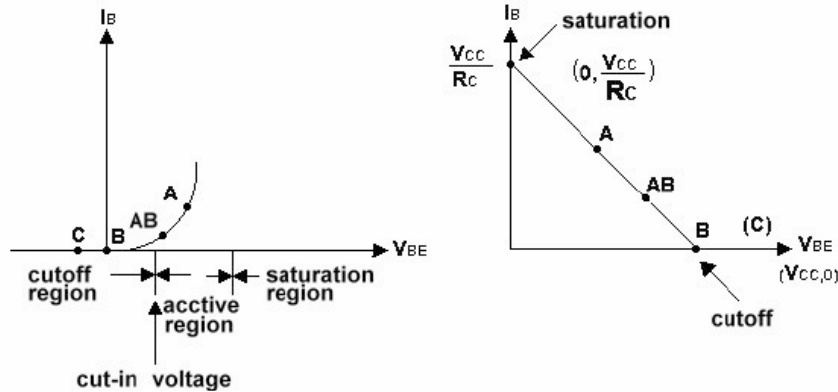


Fig. 5.4

☞ Effect of Q point to amplifying circuit

(1) The DC bias circuit of the transistor circuit is designed in accordance with the amplification class (class A, B, AB and C) of the transistor. The locations of Q point for each amplification class is respectively shown in Fig 6.5.



**Fig. 5.5**

Among them,

- Class A: The operating point is designed in the center point of the straight line portion of the characteristic curve.
- Class B: The operating point is designed in the cutoff point in which  $V_{be} = 0$ .
- Class C: The operating point is designed below the cutoff point, and  $V_{be}$  is negative.
- Class AB: The operating point is designed between that of Class A and Class B.

(2) The location of the operating point will determine the maximum output voltage. The operating point shall be designed in accordance with the strength of the input signal  $I_b$ , as shown in Fig 5.6. From Fig 5.6, we can find:

- For the circuit with larger input signal, the operating point shall be designed in the center point of the load line ( $V_{ce} = 1/2 V_{cc}$ ) as shown in Fig 5.6 (a).
- If the input signal is smaller, the operating point can be designed in the upper portion as shown in Fig 5.6 (b), or the lower portion as shown in Fig 5.6 (c).
- If the operating point is not designed in the center of the load line, the output waveform will generate the distortion shown in Fig 5.7 (a) or (b) when the input signal is larger, wherein the peak will be clipped in this distortion.
- Although the operating point is designed in the center of the load line, the distortion that will clip the peaks of both positive and negative half cycle will be generated as shown in Fig 5.8 when the input signal is very large. The only way to eliminate this distortion shown in Fig 5.8 is to raise  $V_{cc}$ .

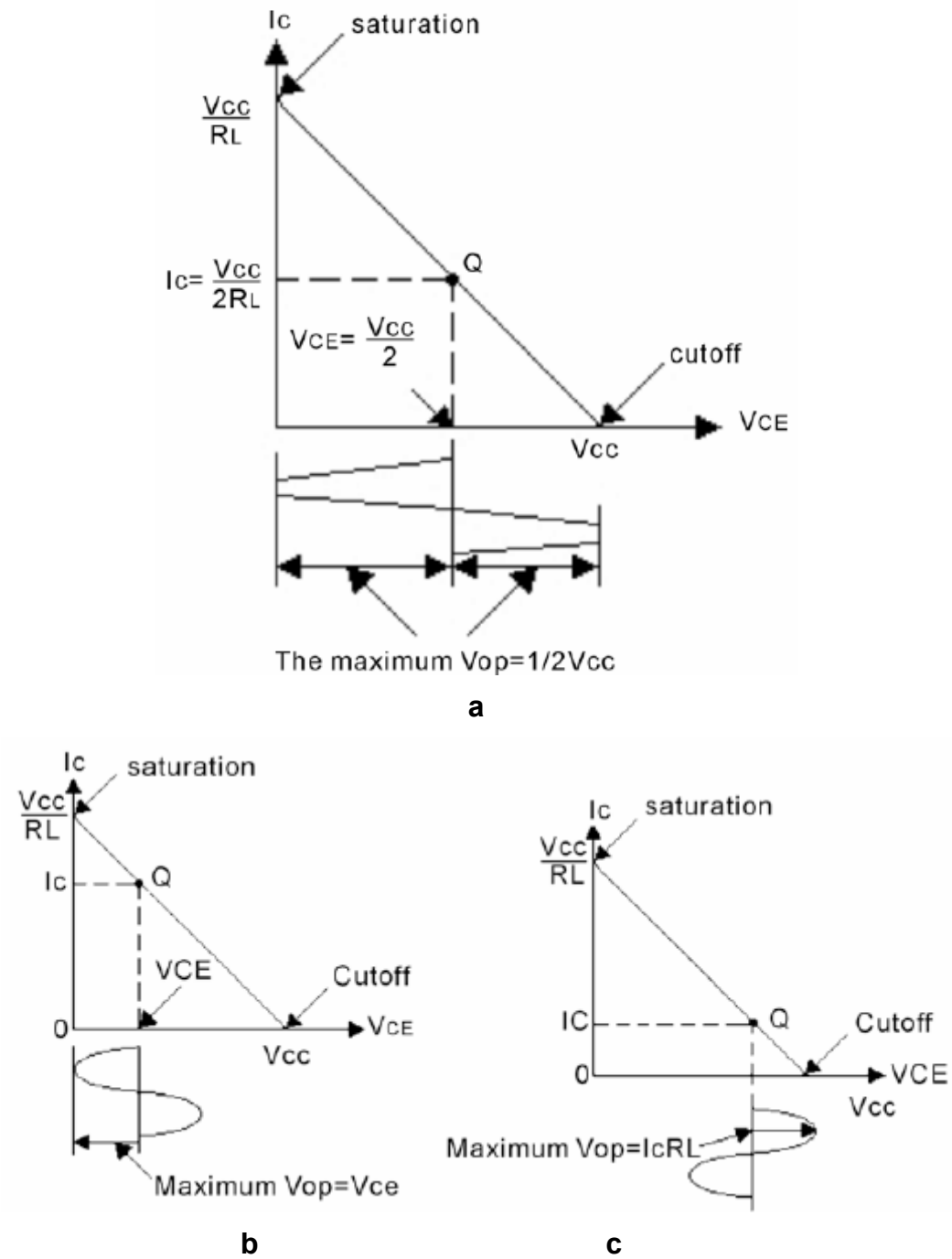
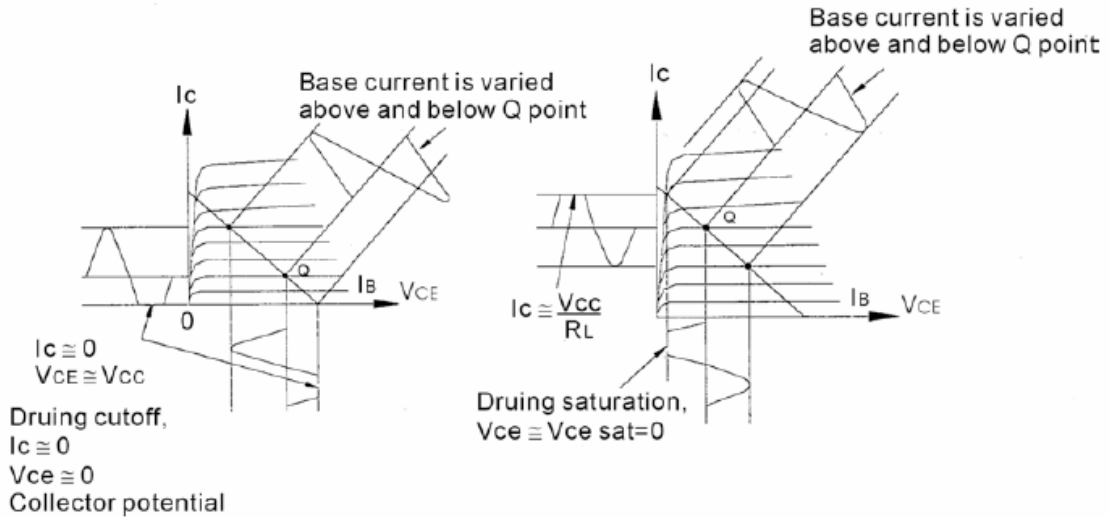
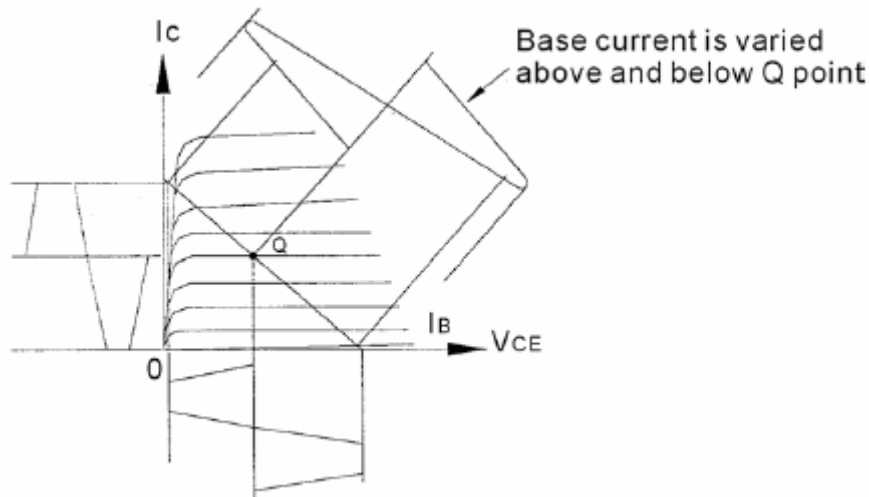


Fig. 5.6



**Fig. 5.7 The distortions caused by inadequate operating point**



**Fig. 5.8 Distortions caused by excessive input voltage**

☞ Drawback of fixed bias circuit

The operating point ( $V_{ce}$ ,  $I_c$ ) of the fixed bias circuit will depend on the magnitude of  $\beta$  ( $I_c = \beta \cdot I_b$ ,  $V_{ce} = V_{cc} - I_c R_c$ ). The magnitude of  $\beta$  will be varied if the transistors are different. If a different transistor is used (although the type No. of the transistor may be same and may be supplied by same manufacturer, the  $\beta$  value of each transistor may not be same), the location of operating point may be varied due to the difference of  $\beta$  value. The operation status of overall circuit will not conform to the original design. Furthermore, the output waveform will be distorted, and the quiescent current will get larger, which may result in the burning own of the transistor.

## B. DC Bias circuit independent of $\beta$ value.

After the design of this circuit has been completed, the operating point will be fixed and will not be shifted due to the difference of  $\beta$  value. As this circuit has the characteristics to automatically lock its operating point, this circuit is also called "self-bias circuit".

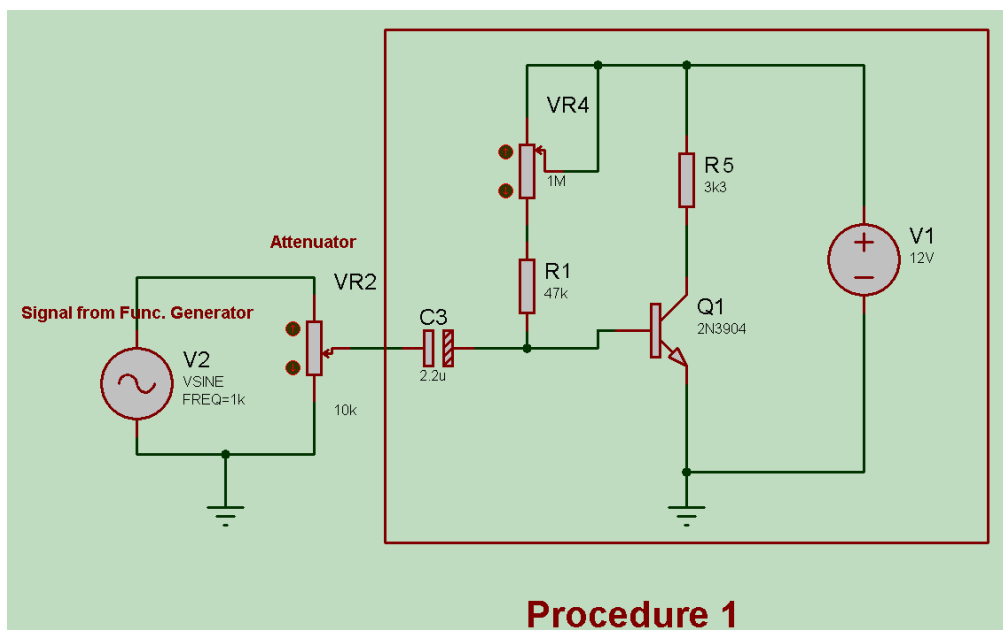
## 5.3 Experiment Equipments

1. KL- 200 Linear Circuit Lab. Device
2. Experiment Module: KL-23001
3. Experiment Instruments: Oscilloscope, Multimeter
4. Connection cables and short-circuit clips

## 5.4 Procedures

### Procedure 1: CE amplifier - fixed bias

- ( 1 ) Firstly fix the module KL-23003 in the KL-200 Linear Circuit Lab, then locate the block marked 23003-block a.



**Fig. 5.9**

- ( 2 ) Insert the short-circuit clips by referring to Fig 5.9.

- ( 3 ) Adjust VR4 and use voltmeter to measure  $V_{CE}$  (out) so that  $V_{CE} = 6V$ , then measure and record value of VR4 (Compare this value with Prelab results).

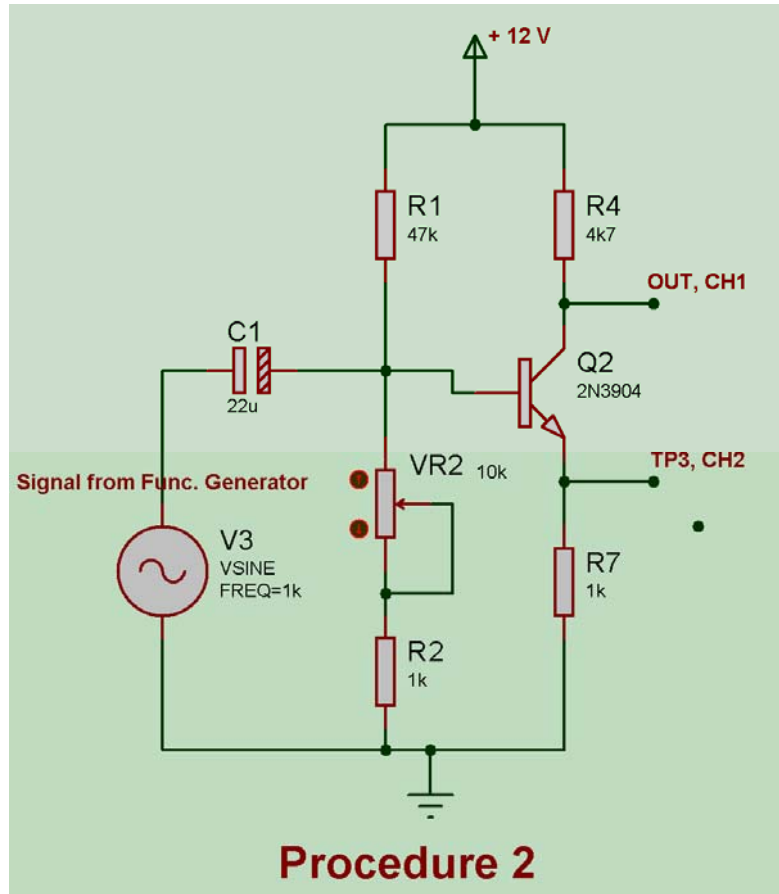
- ( 4 ) Measure  $I_{BQ}$  and  $I_{CQ}$  and calculate  $\beta_{DC}$ .
- ( 5 ) Connect signal generator in the input terminal (IN) and connect oscilloscope to the output terminal (OUT)
- ( 6 ) Adjust signal generator to 1kHz and increase the input amplitude until output the oscilloscope displays maximum non-distorted waveform. **You will notice that minumum voltage amplitude available (which is approx. 130 mV(p-p) ) is not low enough. So use an attenuator (VR2).**
- ( 7 ) When the maximum non-distorted waveform is generated in OUT, use oscilloscope to measure input and output signal amplitudes, then make records.
- ( 8 ) Calculate the gain of the amplifier.

$V_{CE}$	6V
<b>VR<sub>4</sub> value</b>	
$I_{CQ}$	
$I_{BQ}$	
$\beta_{DC}$ (calculated)	
Maximum input signal amplitude V(p-p)	
Resulting output signal amplitude V(p-p)	
Gain, $A_v$	

**Table 5.1**

**Procedure 2: CE amplifier – bias independent of  $\beta$  value**

**( 1 )** Insert the short-circuit clips by referring to Fig 5.10.



**Fig. 5.10**

**( 2 )** Connect ammeter to measure  $I_{BQ}$ ,  $I_{CQ}$ .

**( 3 )** Adjust VR2 (10K) so that  $V_C$  (out) =  $1/2 V_{CC}$ , then measure the value of VR2.

**( 4 )** Measure  $I_{BQ}$ ,  $I_{CQ}$ .

**( 5 )** Connect signal generator in the input terminal (IN) and connect oscilloscope CH1 to the output terminal (OUT, TP5), adjust the signal generator amplitude so that the oscilloscope can display maximum non-distorted waveform @ 1kHz at output terminal.

**( 6 )** Connect oscilloscope CH2 to TP3 (Emitter pin).

- (7) Using the "MATH" operator of the oscilloscope, obtain the graph of CH1-CH2 which equals  $V_C - V_E = V_{CE}$ .
- (8) For this state, measure the maximum output voltage swing.
- (9) With the obtained values, fill the desired values in Fig. 5.11.

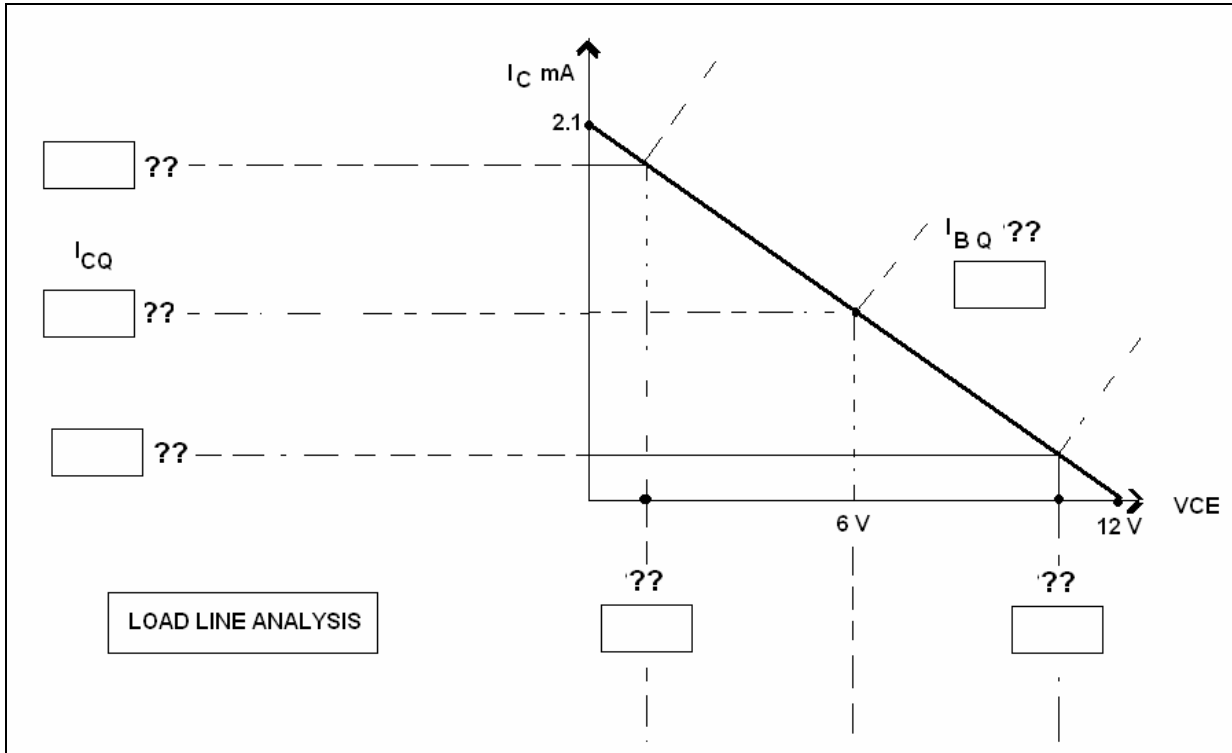


Fig. 5.11